

AM2861 H-Bridge Brushed DC Motor Driver

● Features and Benefits

- 1) Operation Voltage Range : 4V to 33V
- 2) Lowest $R_{DS(ON)}$: HS +LS = 115m Ω
- 3) 3A Continuous Current, 5A Peak Current
- 4) Over Temperature Protection
- 5) Over Current Protection
- 6) Low Standby Current < 2uA
- 7) Low Quiescent Current
- 8) SOP-8 Package For Small Size PCB Layout

● Applications

- Robotics
- AI Home Appliances
- Robot Vacuum
- Electric Curtain
- Servo Motor
- Industrial Equipment
- Other Mechatronic Applications
- DC Brushed Motor Drive

● Description

AM2861 is a brushed DC motor driver IC, provides outside PWM pulse to control motor speed, and it drives current capability up to 3A continuous and 5A peak.

The device provides well protections for motor and device itself including internal functions for overcurrent and over temperature protection.

● Ordering Information

| Orderable Part Number | Package | Marking |
|-----------------------|---------|---------|
| AM2861 | SOP-8 | AM2861 |

● **Absolute Maximum Ratings ($T_A=25^\circ\text{C}$)**

| Parameter | Symbol | Limits | Unit |
|-----------------------------|---------------|-----------|------------------|
| Power Supply Voltage | VCC | 42 | V |
| Input IN_A and IN_B Voltage | V_{IN_X} | -0.3 to 6 | V |
| Peak Current | I_{O_peak} | 5 | A |
| Operating Temperature Range | T_{opr} | -40~+125 | $^\circ\text{C}$ |
| Storage Temperature Range | T_{stg} | -40~+150 | $^\circ\text{C}$ |

● **ESD Ratings**

| | | Value | Unit |
|-----------------------------------|---------------------------------------|-------|------|
| V_{ESD} Electrostatic discharge | Human-body model (HBM) ⁽¹⁾ | ±8000 | V |
| | Machine model (MM) ⁽¹⁾ | ±400 | V |

(1) The test method refers to JEDEC EIA/JESD22-A114-B.

● **Recommended Operating Conditions ($T_A=25^\circ\text{C}$)**

(Set the power supply voltage taking allowable dissipation into considering)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|----------------------------------|-------------|------|------|------------------|------|
| Power Supply Voltage | VCC | 4 | | 33 | V |
| Input IN_A and IN_B Voltage | V_{IN_X} | -0.3 | | 6 ⁽¹⁾ | V |
| H-Bridge Output Current | I_{OUT} | | | 3 ⁽²⁾ | A |
| Externally Applied PWM Frequency | F_{IN_X} | | | 30 | KHz |

(1) Input signal voltage does not be higher than VCC voltage.

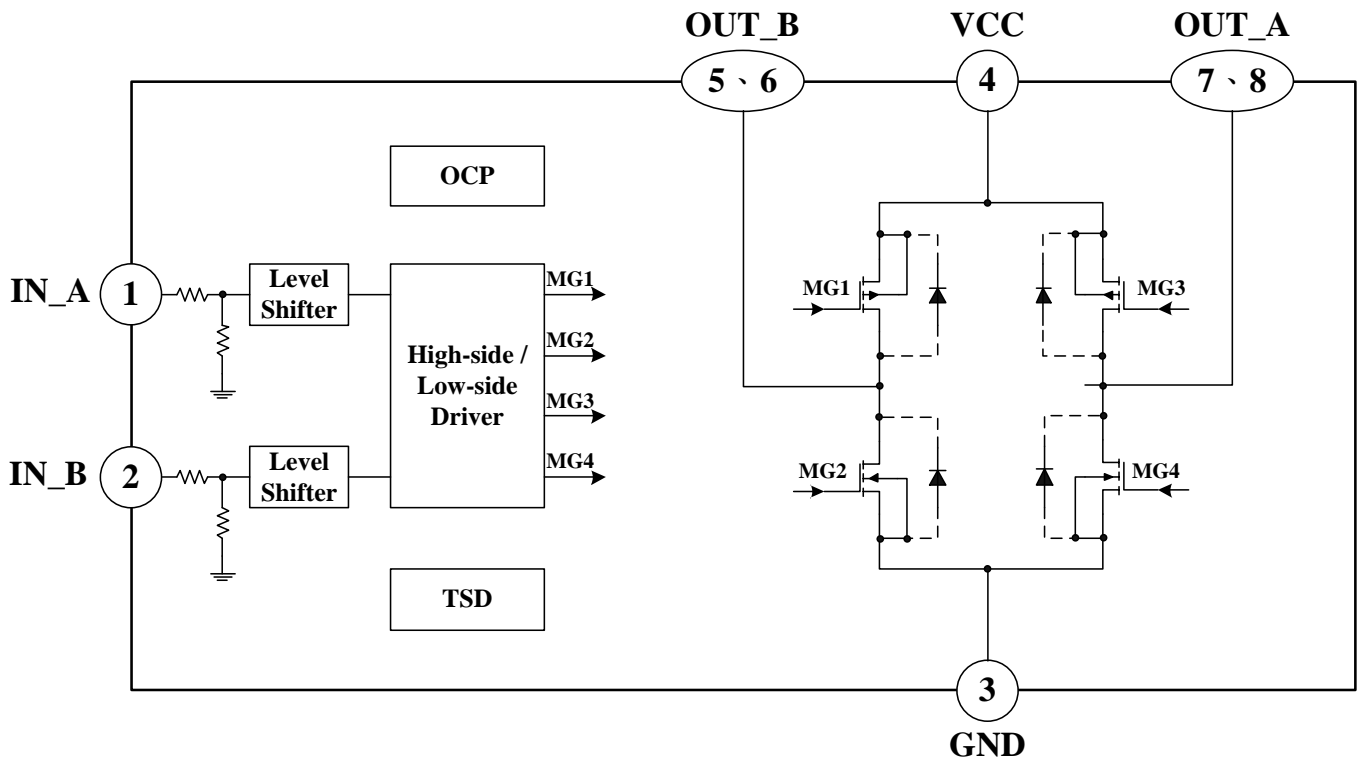
(2) Power dissipation and thermal limits must be observed

● Electrical Characteristics (Unless otherwise specified, $T_A = 25^{\circ}\text{C}$, $V_{CC}=6\text{V}$)

| Parameter | Symbol | Limit | | | Unit | Conditions |
|------------------------------------|--------------|-------|------|------|--------------------|-----------------------------------------------|
| | | Min. | Typ. | Max. | | |
| Power Supply | | | | | | |
| Supply Current | I_{CC} | | 4 | | mA | IN_A/B= L/H or H/L or H/H No load on OUT_A/B, |
| Standby Current | I_{STB} | | | 2 | uA | IN_A/B= L/L |
| IN_X Inputs | | | | | | |
| Input H level Voltage | V_{IN_XH} | 2.0 | | 6 | V | |
| Input L level Voltage | V_{IN_XL} | -0.3 | | 0.7 | V | |
| Input H level Current | I_{IN_X} | | 100 | | μA | $V_{CC} = 6\text{V}$, $V_{IN} = 3\text{V}$ |
| Input Frequency | F_{IN_X} | | | 30 | KHz | |
| Input Pulldown Resistance | R_{IN_X} | | 30 | | K Ω | |
| H-Bridge FETs | | | | | | |
| On-Resistance | $R_{DS(ON)}$ | | 115 | | m Ω | $I_o = 1\text{A}$ Upper and Lower total |
| On-Resistance | $R_{DS(ON)}$ | | 130 | | m Ω | $I_o = 3\text{A}$ Upper and Lower total |
| Overcurrent Protection | | | | | | |
| Overcurrent Trip Level | I_{OCP} | | 5 | | A | |
| Thermal Shutdown Protection | | | | | | |
| Thermal Shutdown Temperature | TSD_P | | 160 | | $^{\circ}\text{C}$ | *1 |
| Thermal Shutdown Release | TSD_R | | 105 | | $^{\circ}\text{C}$ | *1 |

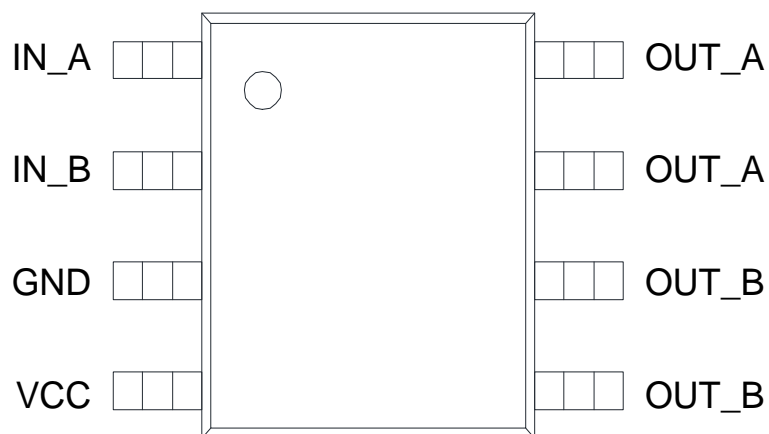
*1: It is design target, not to be measured at production test.

● Block Diagram



● Pin configuration SOP-8

Top View



● Pin Descriptions

| PIN No. | Pin Name | I/O | Description |
|---------|----------|-----|-------------------|
| 1 | IN_A | I | Logic Input A |
| 2 | IN_B | I | Logic Input B |
| 3 | GND | I | Ground Pin |
| 4 | VCC | I | Power Supply |
| 5 | OUT_B | O | Output Terminal B |
| 6 | OUT_B | O | Output Terminal B |
| 7 | OUT_A | O | Output Terminal A |
| 8 | OUT_A | O | Output Terminal A |

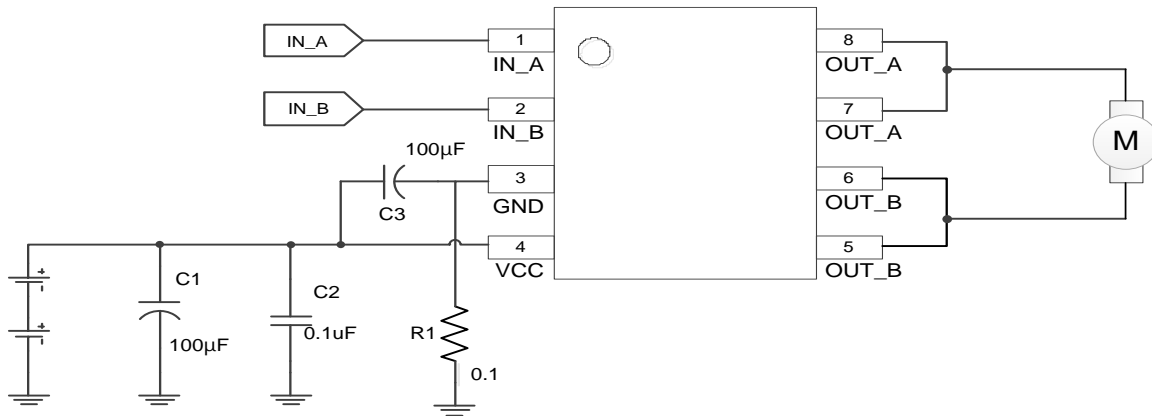
● Input Logic Descriptions

Function Truth Table

| IN_A | IN_B | OUT_A | OUT_B | Mode |
|------|------|---------|---------|---------|
| L | L | High-Z* | High-Z* | Stop |
| L | H | L | H | Reverse |
| H | L | H | L | Forward |
| H | H | L | L | Brake |

Note*: "High-Z" is the status that High-side MOSFETs and Low-side MOSFETs of H-Bridge are switched to "OFF".

● Application:



● Circuit Descriptions

1. C1 、 C2: Power supply VCC pin capacitor:
 - a. The capacitor can reduce the power spike when the motor is in motion, and prevent the IC from being damaged by the VCC peak voltage. They can stabilize the power supply voltage and reduce its ripples.
 - b. The C1 capacitor can compensate power when motor starts running.
 - c. The capacitor value (uF) determines the stability of the VCC during motor in motion. If the large voltage power or a heavier loading motor is used, then a larger capacitor would be needed.
 - d. On the PCB configuration, the C1 、 C2 must be placed as close as possible to VCC pin.

2. If the C3 layout location is away from the VCC power line or the R1 resistor value is larger than 100mΩ, the C3 capacitors 100µF or is highly recommended to be placed in parallel with AM2861 VCC to GND; the capacitor layout location should be placed as close as practicable to AM2861. Please refer to above application circuit diagram, it is to suppress sampling resistor R1 ground noise to ensure MCU ADC detect sampling voltage precisely.

3. It's not allowed INA, INB input remain floating status, because there is a minor leakage current between P-N junction when temperature rising, the leakage current will go through internal pull- low resistor which causes INA or INB floating level abnormal pull high and output abnormal working.

4. GND Pin (GND):

When current sense (sampling resistor) is used, to feedback sampling voltage to MCU precisely, please refer to following suggestion to get optimal performance:

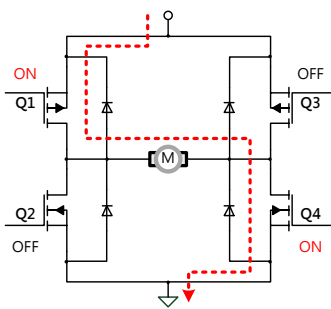
In order to use PWM current control, a low-value resistor (R1) less than 100mΩ is placed between the GND pin for current sensing purposes. The ground-trace should be as short as possible. For low-value sense resistors, the ground-trace voltage drops in the PCB can be significant, and should be taken into account.

When selecting a value for the sense resistor, be sure not to exceed the maximum voltage on the GND pin of ±250 mV at maximum load. During over-current events, this rating may be exceeded for short durations.

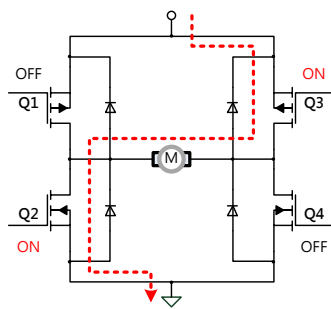
The resistance of the sense resistor must be rated for high enough power.

● Operating Mode Descriptions

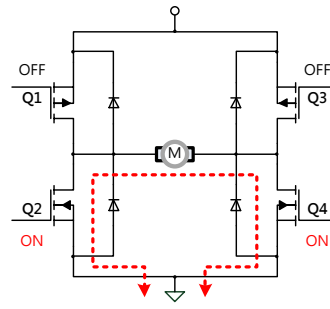
- a) Forward mode: When $IN_A=H$, $IN_B=L$, then $OUT_A=H$, $OUT_B=L$
- b) Reverse mode: When $IN_A=L$, $IN_B=H$, then $OUT_A=L$, $OUT_B=H$
- c) Brake mode: When $IN_A=IN_B=H$, then $OUT_A=OUT_B=L$
- d) Stop mode: When $IN_A=IN_B=L$, then $OUT_A=OUT_B=Hi-Z$



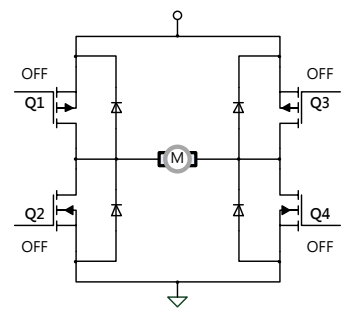
a) Forward mode



b) Reverse mode



c) Brake mode



d) Stop mode

● Protection Mechanisms Descriptions

1) Over-current protection (OCP)

When the IC conducts a large current, 5A (Typ), the internal overcurrent protection will be triggered. The device enters protection mode and disables partial MOSFETs in the H-Bridge to avoid damaging IC and system. The device operation resumes when the current falls below safe range. If the overcurrent protection is still be triggered, the cycle repeats.

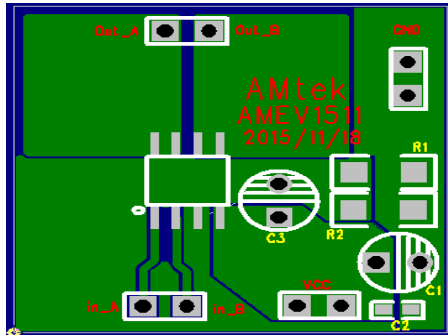
2) Over-temperature protection

If the IC junction temperature exceeds 160°C (Typ.), the internal thermal shutdown protection will be triggered, and then partial FETs in the H-Bridge are disabled so that it will ensure the safety of customers' products. If the IC junction temperature falls to 105 °C (Typ.), the IC resumes automatically.

● Layout Guidelines

1. Layout Example

PCB Size 25x25 mm² \ single side



Top Layer

2. Layout Consideration

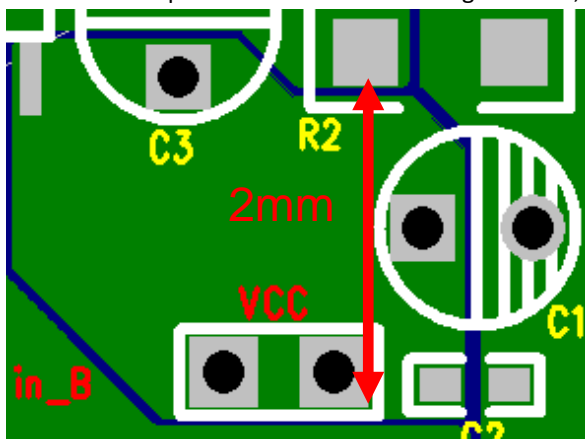
The layout is very important when designing high current and high frequency switching converters. Layout will affect noise pickup. Correctly layout can realize a good design with less background noise. Make all the connections for the power components in the top layer with wide copper filled areas or polygons. In general, it is desirable to make proper use of GND planes and polygons for power distribution and heat dissipation.

3. Power trace

3.1 Power trace (VCC) should be as short as possible.

3.2 On the PCB configuration, the C1 and C2 must be mounted as close as possible to VCC pin in order to reduce EMI noise.

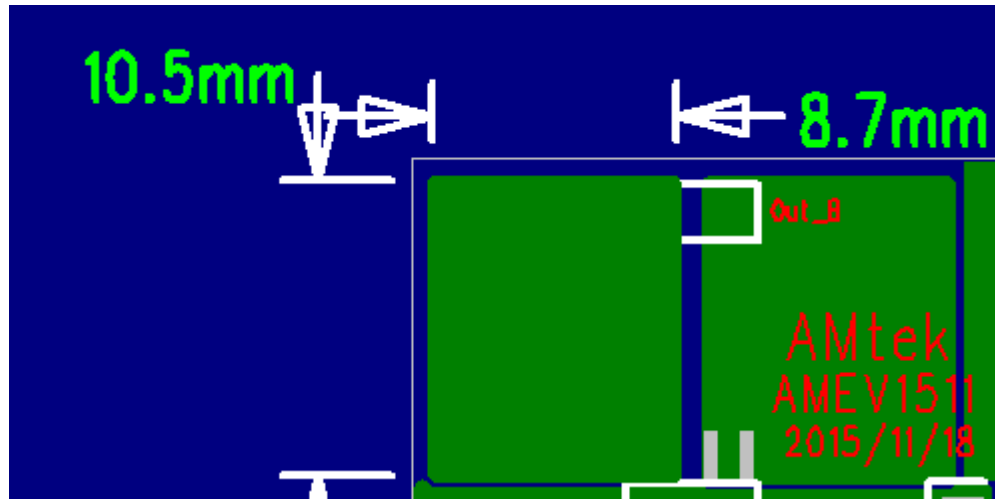
3.3 To ensure that power trace can conduct high current, the width of power trace should be wider than 2 mm.



4. OUTPUT

4.1 OUT_A and OUT_B trace width need at least 2mm for high current going through.

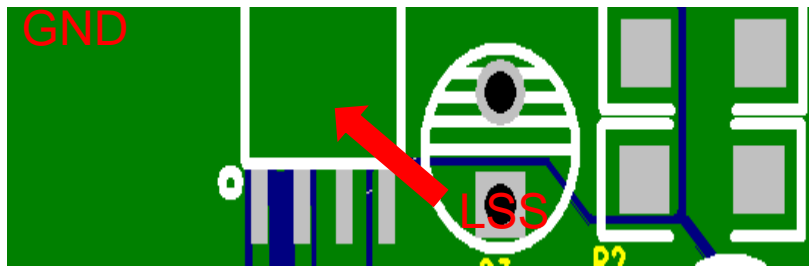
4.2 For OUT_A & OUT_B thermal design consideration, it should be big one piece of copper (for example: 10.8mm x 5.1mm) without any gaps.



TOP layer

5. GND

GND is a high-current path through the motor driver. The width of connecting metal trace should be as wide as possible.



TOP layer

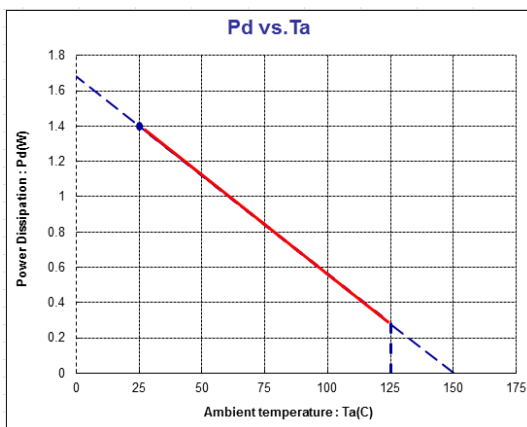
● Thermal Information

| | | |
|---------------|--------------------------------------------|----------|
| θ_{ja} | junction-to-ambient thermal resistance | 89.2°C/W |
| Ψ_{jt} | junction-to-top characterization parameter | 10.6°C/W |

Condition :

- FR4 PCB 25 x 25 mm²
- 1S1P-2 layers
- with 1 oz copper

● Power Dissipation



● How to predict Tj in the environment of the actual PCB

Step 1: Use the simulated Ψ_{jt} value listed above.

Step 2: Measure Tt value by using ~40 gauge thermocouple or thermo gun.

Tt : Temp. at top center of the package

Step 3: calculate power dissipation

$$P \cong (VCC - |V_{O_Hi} - V_{O_Li}|) \times I_{OUT} + VCC \times I_{cc}$$

Step 4: Estimate Tj value

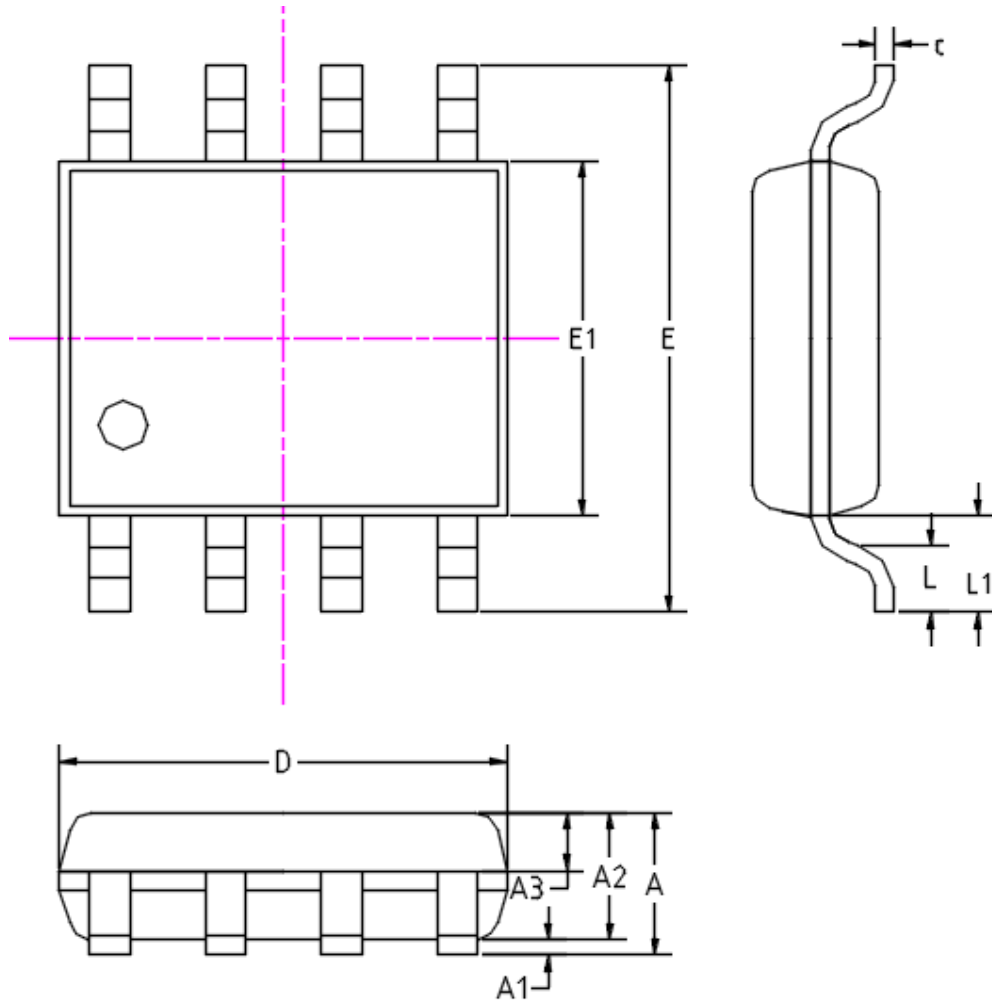
$$T_j = T_t + \Psi_{jt} \times P$$

Step 5: Calculate θ_{ja} value of actual PCB

$$\theta_{ja} = \frac{(T_j - T_a)}{P} = \frac{T_t + \Psi_{jt} \times P - T_a}{P} = \frac{T_t - T_a}{P} + \Psi_{jt}$$

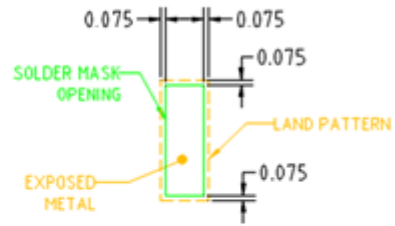
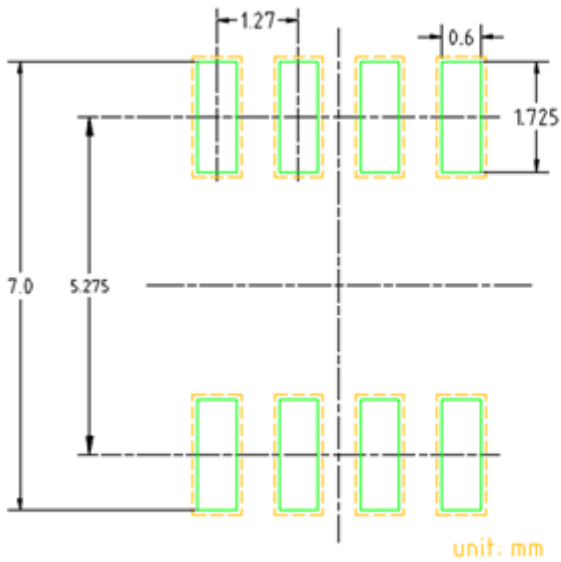
● Packaging outline --- SOP-8

Unit: mm



| SYMBOL | MILLIMETERS | | INCHES | |
|--------|-------------|------|------------|-------|
| | Min. | Max. | Min. | Max. |
| A | -- | 1.75 | -- | 0.069 |
| A1 | 0.10 | 0.25 | 0.004 | 0.010 |
| A2 | 1.25 | 1.65 | 0.049 | 0.065 |
| A3 | 0.50 | 0.70 | 0.020 | 0.028 |
| b | 0.39 | 0.49 | 0.015 | 0.190 |
| c | 0.10 | 0.25 | 0.004 | 0.010 |
| D | 4.80 | 5.00 | 0.189 | 0.197 |
| E | 5.90 | 6.10 | 0.232 | 0.240 |
| E1 | 3.80 | 4.00 | 0.150 | 0.157 |
| e | 1.27 TYP. | | 0.05 TYP. | |
| L | 0.45 | 1.00 | 0.018 | 0.039 |
| L1 | 1.10 TYP | | 0.043 TYP. | |

● Land Pattern And Solder Mask



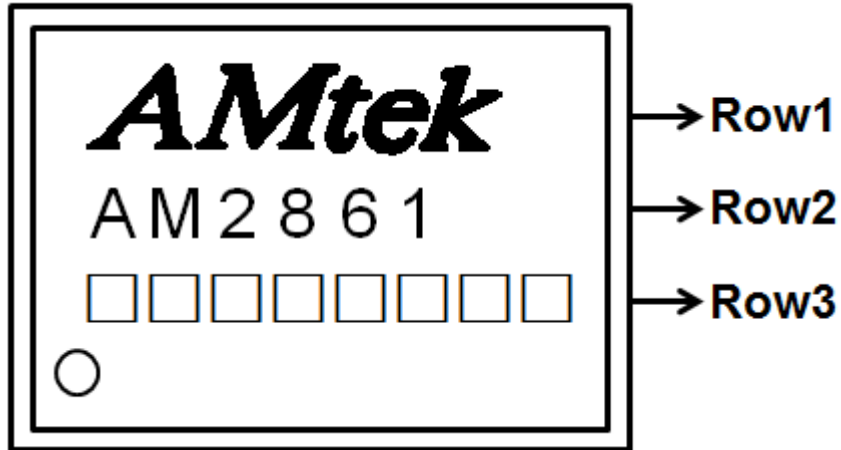
Solder Mask Define

SOP-8 LAND PATTERN

● **Marking Identification**

Package Type : SOP8

Device : AM2861

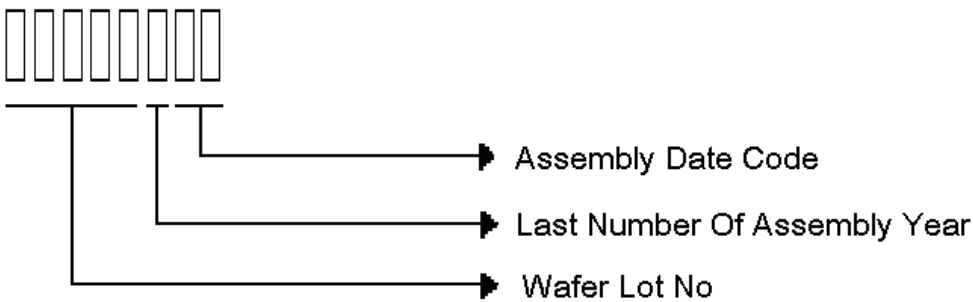


NOTE:

Row1 : Logo

Row2 : Device Name

Row3 : Wafer Lot No use five codes + Assembly Year use one code + Assembly Week use two codes



Example: Wafer Lot No is EB168 + Year 2017 is H + Week 08 is 08 , then mark "EB168H08"

The last code of assembly year, explanation as below: :

(Year : A=0,B=1,C=2,D=3,E=4,F=5,G=6,H=7,I=8,J=9. For example: year 2017=H)

● Revision History

| Date | Revision | Changes |
|-------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 9.Oct.2018 | V1.0 | New release |
| 13.Nov.2018 | V1.1 | P2. Operate voltage range change to 3.6 ~33V P3. OCP retry time chage to 0.5ms P8. Add layout Guideline |
| 3.Jun.2019 | V1.2 | P1. Add overcurrent protection P3. Input low level range change to -0.3 ~ 0.7V P4. Revise Block Diagram |
| 3.Nov.2020 | V1.3 | P2. Operate voltage range change to 4 ~33V P3. Remove deglitch time and retry time |
| 29.Sep.2022 | V1.4 | P2. Operating Temperature Range change to -40°C ~ 125°C Add ESD Rating P3. Add overcurrent Protection P10. Revise Power Dissipation P11. POD update P12. Add Land pattern and solder mask P14. Add Revision History |

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